REMARKS

Claims 1-4, 6-8, 16-20, and 23-24 are amended herein. Claims 15, 21, and 22 are cancelled herein. Claims 16-20, and 23-25 remain pending in the case.

102(e) Rejection

Claims 1-18, 21, 22, 24, and 25

In the Office Action, the Examiner rejected Claims 1-18, 21, 22, 24, and 25 under 35 USC 102(e) as being anticipated by Triece et al. (US 2003/0005254 A1). Applicant has reviewed the Triece et al. reference and respectfully asserts that the claimed embodiments of the present invention are not anticipated by Triece et al. for the following rationale.

Applicant respectfully states that Independent Claim 1 recites the features of "a plurality of variable width memory locations coupled to said bus, said plurality of variable width memory locations having various bit widths to store information, wherein said plurality of variable width memory locations receive a number of bits corresponding to the width of the variable memory locations (emphasis added)." Support for the Claim amendment can be found throughout the present application including Figure 1.

Applicant further states that the description and utilization of variable width memory locations as stated in the specification and shown in Figure 1 is clearly defined. For example, on page 12 line 34, "a memory location is assigned a width based on the identifiers portions of number of bits. If the number of bits in the identifier portion is 10, then a memory location is programmatically

assigned a width of ten bits. Furthermore, as each portion of bits is identified, a memory location is allocated a correlating storage size. If the number of bits is five then a second memory location is allocated a storage capacity of five bits." Therefore, due to the varying widths of the memory location or locations, the identified portions of bits will fit into each memory location without overfilling or under filling the memory location.

Applicant understands this method of variable width memory locations to be inherently different from the memory allocation taught by Triece et al. That is, Applicant understands Triece et al. to teach the use of a data memory of any convenient size, e.g., a 64k-bit memory array having a 4K bit x 16 bit arrangement. This method taught by Triece et al. and understood by the Applicant would have the same problems as stated in the background of the present Application. Specifically, "memories having uniform memory widths are often underutilized and filled with superfluous filler bits causing processor slowdown." Triece et al. do not teach nor anticipate the solution to this underutilization of memory locations.

Therefore, Applicant respectfully submits that Triece et al. neither anticipates nor suggests the present claimed invention as recited in Independent Claim 1, and as such, Claim 1 overcomes the 35USC 102(e) rejection of record. Accordingly, Applicant respectfully submits that Triece et al. also does not anticipate nor suggest the present claimed invention as recited in Claims 2 through 7 which depend from Independent Claim 1 and that these Claims are also in a condition for allowance as being dependent on an allowable base Claim.

With respect to Claim 8, Applicant respectfully states that Independent Claim 8 recites the features of "wherein said memory cell is allocated a storage size correlating to the bit capacity of said register." Support for the Claim amendment can be found throughout the present application including Figure 1 and page 13 of the Specification.

Applicant further states that the description and utilization of variable width memory locations as stated in the specification and shown in Figure 1 is clearly defined. For example, on page 12 line 34, "a memory location is assigned a width based on the identifiers portions of number of bits. If the number of bits in the identifier portion is 10, then a memory location is programmatically assigned a width of ten bits. Furthermore, as each portion of bits is identified, a memory location is allocated a correlating storage size. If the number of bits is five then a second memory location is allocated a storage capacity of five bits." Therefore, due to the varying widths of the memory location or locations, the identified portions of bits will fit into each memory location without overfilling or under filling the memory location.

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are often underutilized and filled with superfluous filler bits causing processor slowdown." Triece et al. do not teach nor anticipate the solution to this underutilization of memory locations.

Therefore, Applicant respectfully submits that Triece et al. neither anticipates nor suggests the present claimed invention as recited in Independent Claim 8, and as such, Claim 8 overcomes the 35USC 102(e) rejection of record. Accordingly, Applicant respectfully submits that Triece et al. also does not anticipate nor suggest the present claimed invention as recited in Claims 9 through 14 which depend from Independent Claim 8 and that these Claims are also in a condition for allowance as being dependent on an allowable base Claim.

Applicant respectfully states that amended Independent Claim 20 recites the features of "wherein said data block is arranged in accordance with a communications packet configuration specification." As the Examiner has stated, the prior art of record does not disclose the above stated feature.

Applicant agrees that the prior art of record neither anticipates nor suggests the present claimed invention as recited in Independent Claim 20. Accordingly, Applicant respectfully submits that the prior art of record also does not anticipate nor suggest the present claimed invention as recited in Claims 16 through 19 which depend from Independent Claim 20 and that these Claims are also in a condition for allowance as being dependent on an allowable base Claim.

Applicant respectfully states that amended Independent Claim 23 recites the features of "means for storing said information returns a number of bits equal to the width of one of said uniquely identifiable different width memory locations in response to a read request." As the Examiner has stated, the prior art of record does not disclose the above stated feature.

Applicant agrees that the prior art of record neither anticipates nor suggests the present claimed invention as recited in Independent Claim 23. Accordingly, Applicant respectfully submits that the prior art of record also does not anticipate nor suggest the present claimed invention as recited in Claims 24 through 25 which depend from Independent Claim 23 and that these Claims are also in a condition for allowance as being dependent on an allowable base Claim.

CONCLUSION

In light of the above amendments and remarks, Applicant wishes to thank the Examiner for the allowance of Claims 20 and 23 if rewritten in independent form including all of the limitations of the base Claim and any intervening Claims. Furthermore, Applicant respectfully requests reconsideration of the rejected Claims 1-14, 16-19, and 24-25.

Based on the amendments herein and the argument presented above, Applicant respectfully asserts that Claims 1-14, 16-20, and 23-25 overcome the rejections of record and, therefore, allowance of these Claims is respectfully solicited.

The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,

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Date:_____

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